UNITED STATES UTILITY PATENT APPLICATION

FOR

A Method, System, and Apparatus

for an Adaptive Weighted Arbiter

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BACKGROUND

1. Field

The present disclosure pertains to the field of computer chip design. More particularly, the present disclosure pertains to a new method, system, and apparatus for an adaptive weighted arbiter.

[0001] 2. Description of Related Art

[0002] Typically, electronic systems include an arbitration logic for arbitrating between requests received from the multiple requesting agents, and for granting access to a resource to a selected one of the requesting agents. For example, a requesting agent may be a modem, keyboard, video controller, serial port, or PCMCIA card, SONET interface, Ethernet Interface, content processor, encryption device, or compression device. and a resource may be an interconnect bus, memory unit, or output buffer. In some situations, such as, peer-to-peer systems, the device may be either the requesting agent and/or the arbitrated resource.

[0003] Present arbitration schemes include round-robin arbiters that are based at least in part on a scheduling algorithm that creates a list of all possible requesting agents ("bidders"). Next, the arbiter assigns a window of time fixed bidding opportunities for each bidder into a table. The arbiter then traverses the table and determines whether the particular bidder is requesting access to the resource. If so, the arbiter grants access to that particular bidder. Otherwise, the arbiter proceeds to the next bidder in the list entry in the table. However, the present round-robin arbiter does not account for past arbitration events. Furthermore, a fixed scheduling algorithm may require bidders to wait for their particular window of time ("time slice") fixed bidding opportunity in the table.

Brief Description of the Figures

[0004] The present invention is illustrated by way of example and not limitation in the Figures of the accompanying drawings.

[0005] Figure 1 illustrates a schematic diagram utilized in accordance with an embodiment.

[0006] Figure 2 illustrates a flowchart for a method utilized in accordance with an embodiment.

[0007] Figure 3 illustrates a system in accordance with one embodiment.

Detailed Description

[0008] The following description provides method and apparatus for improved multi-core processor performance despite power constraints. In the following description, numerous specific details are set forth in order to provide a more thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the invention may be practiced without such specific details. Those of ordinary skill in the art, with the included descriptions, will be able to implement appropriate logic circuits without undue experimentation.

[0009] As previously described, a problem exists for round robin arbiters. In contrast to the prior art, the claimed subject matter facilitates a novel adaptive weighted arbitration algorithm that is user configurable. Also, the claimed subject matter allows the arbiter to consider past arbitration history events and is dynamic to allow for losing bidders to increase their probability of being selected to access the resource. The arbitration algorithm, circuitry, and system will be discussed further in connection with Figures 1-3.

[0010] Figure 1 illustrates a schematic diagram utilized in accordance with an embodiment. In one embodiment, the schematic depicts an adaptive weighted arbiter. In another embodiment, the adaptive weighted arbiter may be utilized as an adaptive weighted round-robin arbiter. In various embodiments, the arbiter may be incorporated within a chipset, a microcontroller, application specific integrated circuit (ASIC), or a processor. Also, the respective weight and accumulator values are flexible because they are user configurable and may be stored in the respective register depicted as 104 for the

weight value and account for past bidding win/loss history or within the accumulator 106.

[0011] The schematic includes a plurality of accumulators 106 that receive a plurality of requests 102 from bidders. In one embodiment, a plurality of n bidders is requesting access to a resource. A comparator is coupled to the plurality of accumulators 106 and generates a grant to one of the bidders based at least in part on a plurality of accumulator values stored within each accumulator.

[0012] In one embodiment, each accumulator stores a single accumulator value and the accumulator value is based at least in part on a user configurable weight value 104. In this same embodiment, the user configurable weight value corresponds to a desired priority for each of the n bidders. For example, in one embodiment, a bidder with a weight value of one indicates a highest priority among the bidders, a bidder with a weight value of two indicates a second highest priority among bidders, etc....

A more detailed explanation of the weighted values, accumulator values, and algorithm will be discussed in connection with Figure 2.

Figure 2 illustrates a flowchart for a method utilized in accordance with an embodiment. In one embodiment, the flowchart depicts a method for an adaptive weight arbitration algorithm that may be implemented in software to control the arbitration logic.

The flowchart depicts one arbitration cycle and may be repeated for subsequent arbitration cycles.

The claimed subject matter facilitates the adaptive weighted arbitration logic by setting n weight values for n bidders, as depicted in a block 202. For example, in one embodiment, the weight value is based on a priority of each of the n bidders. Also, the

algorithm will set n accumulator values for n bidders to a predetermined value within a range of values, as depicted in a block 204. For example, in one embodiment, the predetermined value is at a midpoint of a particular accumulator's range. In one embodiment, all the accumulators will have the same range. Typically, the range will be a power of 2, such as, 8, 16, 32, 64, 128, etc.. For example, an user may select a range based at least in part the desired granularity(accuracy).

For each arbitration cycle, the algorithm declares a winner for one of the n bidders and grants the winning bidder access to the resource based at least in part on the accumulator value, as depicted in a block 206. For example, in one embodiment, the winning bidder has the highest accumulator value as determined by the comparator described in connection with Figure 1. Also, the arbiter algorithm decrements the accumulator value of the winning bidder. For example, the algorithm may decrement the winning bidder's accumulator value by the amount of the bidder's weight value. However, if decrementing the winning bidder's accumulator value would result in a negative value, then, the accumulator value is set to zero.

In one embodiment, the remaining bidders that were contending for the resource during the particular arbitration cycle ("losing bidders") have their respective accumulator values incremented after the winning bidder has been determined, as depicted in a block 208. For example, a losing bidder with an accumulator value between 0-25% quartile of their range will have their respective accumulator value increased by a value of four; a losing bidder with an accumulator value between 25-50% quartile of their range will have their respective accumulator value increased by a value of three; a losing bidder with an accumulator value between 50-75% quartile of their range will have their respective

accumulator value increased by a value of two; and a losing bidder with an accumulator value between 75-99% quartile of their range will have their respective accumulator value increased by a value of one. Therefore, the claimed subject matter allows the arbiter to consider past arbitration history events and is dynamic to allow for losing bidders to increase their probability of being selected to access the resource.

However, the claimed subject matter is not limited to the preceding quartiles and increment and decrement values. For example, one skilled in the art appreciates utilizing different increment values and quartile values.

In some embodiments, an accumulator value is unchanged for a losing bidder with an accumulator value at 100% of its respective range.

In one embodiment that supports multiple request/grant interactions, the flowchart depicts a line from 208 back to 206.

Figure 3 illustrates a system in accordance with one embodiment. The system in one embodiment is a processor 302 that is coupled to a chipset 304 that is coupled to a memory 306. For example, the chipset performs and facilitates various operations, such as, memory transactions between the processor and memory. In one embodiment, the system comprises one or all of the previous embodiments for an arbitration algorithm depicted in connection with Figures 1-2. For example, the system may be coupled to a variety of requesting devices and arbitrated resources (as previously described) and incorporates the arbitration schematic and methods described earlier to arbitrate access between the requesting agents and the arbitrated resource.

While certain exemplary embodiments have been described and shown in the

accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art upon studying this disclosure.